Combining the graphical and alphanumerical display on a CRT monitor

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This article deals with the hardware structure and operation of an image processing system built around a ZILOG 2-80 microprocessor, in detail. The picture memory is sized of 256 x 256 x 8. The system consists of two Z-80 uP, one of them has the task of image processing, the other handles an alphanumerical pictorial terminal and controls the camera. The graphical and alphanumerical information are displayed in the same time on the predefined area of the CRT monitor. The system able to control CCD cameras, and to process their visual information.

1. THE DESIGN REQUIRES:

The desired display format is illustrated in the Figure 2b, with the description about the design requires as follows:

The alphanumerical information stored in the alphanumerical display character memory to be displayed on the left rectangular CRT screen portion with the desired maximum number of display characters per a character row to be 14.
The information of the 256 x 256 x 8 format picture to be displayed on the remained CRT screen portion from the special memory called by the name "picture memory" which to be designed so that it to be a common pictorial data storage of the MICRO-computer based parallel pictorial data processing system. In this manner, this require to be understood that the picture memory to be the pictorial data display buffer and also to be shared to use by many other pictorial data requiring sources in which there are the Microprocessors. In this manner the such desired picture memory, to be called by Common Picture Memory and written by symbol CPM.

The CPM to be shared by the following memory request sources:
- One Camera Data Input Controller (CDIC) which is used to select the predesigned pictorial window from the 512 x 512 format picture obtained from the CCD. The predesigned pictorial window to be 256 x 256 format and the input data transmitting timing period to be minimum 2 us per a byte.
- Some of the microprocessor based microcomputers with the predetermined type to be ZILOG Z-80. They need to access the CPM for the purposes of the digital picture processing operations.
- One Picture Display Controller which does to control the pictorial information transferring from the CPM to display on the screen under the format of the bright TV picture. The CRT monitor is selected to be Ball Bross TV-12 12 MHz-BW with the screen refresh rate to be 50 Hz. The specifications for the Ball Bross monitor is shown in the Table 1.

Because of the economical causes and since the practical IC stocking we could have choosen that such desired common picture memory to be designed on the base of using the MOSTEK 16Kx1 Dinamic RAM devices. Since that the problem of memory refreshing must be regarded in the hardware design of CPM as an important problem.

Because of the limiting of the paper, in this article we only discuss the following hardware designing resolutions:
- Applying the INTEL 8275 Programmable CRT Controller to control the nontransparent universal alphanumeric picture displaying process.
- Common Picture Memory designing.

2. THE BASIC HARDWARE DESIGN RESOLUTIONS

2.1 Applying the INTEL 8275 Programmable CRT Controller to control the nontransparent combined alphanumeric picture displaying process.
The INTEL 8275 CRT Programmable Controller provides a number of user programmable display format parameters. Display formats having from 1 to 80 characters per row, 1 to 64 rows per screen, and from 1 to 16 horizontal lines per row are available. Since all just said specifications of 8275's display format controlling ables, hence we can to apply the 8275 to design the Alphanumeric CRT Display Terminal with the display format specifications as follows:

**Screen format (Figure 2.a)**

- 32 character rows per screen
- 80 characters per row

**Character format (Figure 2b)**

- 5x7 character contained within 7x10 matrix, 1st and 10th lines blanked, 1st and 7th columns blanked, 9th line cursor position, blinking under line cursor.

For obtaining such desired display format with the selected Ball Bross CRT monitor having the specifications shown in the Table 1.1 and with the screen refresh rate choosen to be 50 Hz, we have designed the alphanumeric terminal having the block diagram to be shown in the Figure 1b, which has the dot logic circuit and dot timing logic's timing diagram to be shown in the Figure 1c.

The important results obtained from the CRT monitor system timing designing are follows:

- Total screen time = 0.02 ms
  - = 34 character row time
- Character row time = 588,23529 us

The vertical retrace blanking time (VRTC)

\[ VRTC = 2 \times \text{character row time} \]

\[ = 1,1764706 \text{ ms} \]

The total line time = 100 \( \frac{\text{character time}}{\text{line}} \)

\[ = 58,823529 \text{ us} \]

The character time / line = 588,23529 ns

x (notes): The 8275 will be programmed for a Vertical Retrace Row count for 2 and for Horizontal Retrace Character Count for 20

The horizontal retrace time (HRTC) = 20 \( \text{character time/line} \)

\[ = 11,764706 \text{ us} \]

\( \text{Dot time/line} = \frac{1}{2} \times \text{character time/line} = 84.0336 \text{ ns} \)

\( \text{Dot clock frequency} = \frac{1}{\text{dot time/line}} = 11.9 \text{ MHz} \)

System clock frequency = \( 2 \times \text{Dot clock frequency} = 23.8 \text{ MHz} \)
By such CRT system timing design we can to define on the CRT screen an array of 32 character rows and 80 character columns, each of the character rows consists of 10 dot lines and each of the character columns consists of 7 dot columns. The signals HRTC delayed and Dot clock are used to sample the dot lines and the dot columns respectively. On the such obtained character coordinate system, we have coordinated the picture display to the alphanumeric display on one CRT screen by the way, which is discussed in the following discussion:

We used the dot lines and the character columns to define the display screen format. For this purpose, we did to index the array by \( M(\text{dot lines}) \times N(\text{character columns}) \), where: \( M=0,1,\ldots,319 \) (up to down) and \( N=1,2,\ldots,80 \) (left to right). The subarray \( M \times N \), where \( M=0,1,\ldots,319 \) and \( N=1,2,\ldots,14 \), are used to display the alphanumeric information, with the number of the character rows to be 32 and the number of the characters per row to be 14. The 256 x 256 x 8 format picture to be stored in the CPM and to be transferred out from the CPM to the screen to display. That picture to be displayed on the screen under the format of an array of 256 x 256 TV bright pixels, the brightness of each pixel is represented by one byte stored in one predefined address of the CPM. One MK 4116P-2 chip is an array of 128 x 128 x 1 memory bit. To store 64K byte we have to use 32 chips, which are connected so that the memory array to be 4 subarrays of 128x128x8 bit.

We defined that the 256x256x8 format to be desampled on the CRT screen at 256x256 pixels (256 pixel lines x 256 pixel columns), 256 pixel lines to be determined geometrically by 256 designed dot lines, from dot line 0 to dot line 255, 256 pixel columns to be determined by doing to sample 64 character columns, from character column 16 to character column 79, into 256 pixel columns, with 4 pixel columns per each and the distance between any two adjacent pixel columns to be 1/4 of the character column’s width. That means that to display 256 pixels of one line we have to transfer the pictorial information from the CPM to the screen with the rate one byte per 147.05882 ns. The 4116P access time is no suitable to this rate. To resolve all these problems we have used the hardware design resolution which is shown in the Figure (2) and which is described in the following discussion.

In our design, 256 pixels of a picturian line to be read out to display by 64 read times, once 4 bytes to be read out. For each display line, under the control of the LCL / Line Control Logic /, the
DRAC is started to count-up the CCK pulses from state 0 when the 15th CCK comes and stopped at the state 63 until to be load to zero when HRTC delayed to be positive. On the base of using 8 tristate output latch registers such 74LS373 we designed the CPM output logic to perform the logic functions of the latch and the multiplexer. 4 data bytes of one memory word to be latched to resisters A0, A1, A2, A3 respectively of the row address is even (DRO=0) and to be latched to the B0, B1, B2, B3 if the row address is odd (DRO=1). 4 data bytes latched in A0, A1, A2, A3 to be selected out byte after byte sequentially by 4 steps, when DRO=1, and 4 data bytes latched in B0, B1, B2, B3 are selected out similarly when DRO=0.

The CPM is designed so that it to be the dual port common memory, this problem is not discussed here concretly because it to be discussed in the following part. The hardware structure of the CPM is designed so that when it to be used as the pictorial display buffer it to be the memory array of 128 rows and 128 columns of the 4 byte memory words, and when it to be used for other purpose it to be 4 memory blocks, each block to be 128 rows x 128 columns x 1 bit memory array. Just discussed problem is solved by the way showing in the Figure 2. We used 32 MK4116P-2 dynamic RAM chips to construct the CPM with 4 blocks MB0, MB1, MB2, MB3 each block having 8 chips. To address the CPM we have to use 16 address bits, in which 7 bits are used to address 128 rows and 7 bits are used to address 128 columns and 2 bits are used to select 4 blocks. The RAS signal to be used as the chip select signal. The block CRWL (Common Read Write Logic) provides all the needed memory control signals in any mod. In the case the the CPM to be used as pictorial display buffer we not use two block select bits and the signal RAS0, RAS1, RAS2, RAS3 to be the same. Any display read cycle is completely performed in one complete period of the CCK pulse. The FCL (Frame Control Logic) is used to control the pictorial frame display process, which consists of 256 pictorial line displaying processes. The DCAC (Display Column Address Counter) is 8 bit synchronous counter which is designed to count the HRTC delayed pulses with the counting sequence is shown in the Figure 2c. The FCL does to control the counting sequence of the DCAC synchronously to the monitor raster in desired manner.

The OCL (Output Control Logic) is used to generate the output control signals a0, a1, a2, a3, b0, b1, b2, b3 for the register A0, A1, A2, A3, B0, B1, B2, B3 respectively, from the sample timing signals d0, d1, d2, ... d13, CCK and DRO. The timing diagram of the
DSTL is shown in the Figure 1 and the designed timing diagram, of the one line display process is illustrated in the Figure 2a.

2.2 Common Picture Memory designing

In our system design, the CPM is designed to be shared by many memory request sources by the means of the dual port public memory. The Picture Display Controller (PDC) is designed to be one of the memory request sources. In the case the CPM to be shared by only PDC, the pictorial data transfer from the CPM to the screen to be performed completely by the way said in the precious part, and in the case the CPM to be shared by another memory request source that process to be performed by the same way but with some notices to be discussed in this part. To solve the problem of sharing the CPM we used the hardware design resolution which is illustrated in the Figure 2 and which is described in the following discussion:

The CPM to be bus coupled to a memory request source by an it’s own bus coupling port, which consists of two following parts

Address Couple Logic (ACL)
Data Couple Logic (DCL)

The CPM Traffic Controller (CTC) does to control the opening-closing traffic of the ports by applying the request-wait-accept procedure with respect to the asigned priorities of the memory request sources. Based on the memory functions which to be requested from the memory request suorces, the memory request suorces are classified into three classes of:

- read request suorces
- write request suorces
- memory refreshing request suorce.

By such classifying, one microprocessor based microcomputer to be regarded as one read request suorce and one write request suorce. By using the signals MREQ, WR, RD of the Z 80 processor, we designed the Z Read Request (ZRRQ) and Z Write Request (ZWRQ) as follows

\[ ZRRQ = \text{MREQ} \times \text{RD} \quad \text{(active high level)} \]
\[ ZWRQ = \text{MREQ} \times \text{WR} \quad \text{(active high level)} \]

Corresponding to each of the 256 first lines of one monitor raster total screen time, the DDC generates the signal Display Read Request (DRRQ) once, which to be active from the leading edge of 13th CCK pulse to the leading edge of the 80th CCK pulse.

Since the CPM is designed from the MOSTEK MK 4116 P-2 type 16 K x 1
dinamic RAM chips, therefore to refresh all 128 rows within 2 ms, a refresh cycle must be executed every 16 μs for one row refreshing. In our design, the CPM Refresh Controller (CRFC) is regarded as a memory request source which generates the refreshing request signal with the cycle about 16 μs.

Our system is designed with one Camera Data Input Controller (CDIC) which is used to control the CCD camera to transfer the information of one (512 x 512 x 8) picture from the output of it, and which does to select the information of (256 x 256 x 8) format window from the obtained information to write into the CPM with the required write-request cycle to be 2 μs minimum.

As we discussed in the previous part, the CPM is designed so that when it to be shared by PDC then it to be the memory array of 128 rows x 128 columns of 4 byte memory words and when it to be shared by another remained memory request source the it to be 4 memory blocks MB0, MB1, MB2, MB3 with each of these block to be the array of 128 rows x 128 columns of 8 bit bytes. To couple 7 address lines of the CPM to the address buses we used INTEL 3242 chip with the in chip memory refreshing address counter. The address bus of each designed memory request source to be couple to the address inputs of the 3242 via the assigned own address port of the Address Couple Logic (ACL). Here we take the note that one microprocessor to be regarded as two memory request sources, which use commonly only one address bus. Also we remark that the address bus of the PDC has 14 address lines, and the address bus of any remained memory request source has 16 address lines in which 14 address lines are coupled to 14 address inputs of 3242 by two 7 line groups, two remained address lines are used as two block select lines which are coupled to the Common Read Write Controller (CRWC) to spend as two logic variants for generating 4 logic functions $RAS0$, $RAS1$, $RAS2$, $RAS3$. The ACL is designed to be the 4 address ports, in which 1 port is assigned to the address bus of the PDC and, 3 ports are assigned to the address buses of the remained memory request sources (without refreshing source). The ports of the ACL are designed on the base of using the buffer input-tristate output registers, so that the ACL to be the buffer-multiplexer, which selects from 4 address buses one address bus to be coupled to the CPM suitably under the control of the CTC.

Data Couple Logic for the read request sources consists of the following logics:

- Output registers
- Output bus couple ports

8 output registers A0, A1, A2, A3, B0, B1, B2, B3 are designed from 8 x 74 LS 373 (tristate output-latch registers) which are connected as shown in the Figure 3a. When the CPM to be shared by the PDC all of 8 registers are used to buffer the output data to be read from the CPM by the way we discussed in the previous part. When the CPM to be shared by another read request sources only 4 registers A0, A1, A2, A3 are used as output buffers of four memory blocks MB0, MB1, MB2, MB3 respectively and they are used as the byte multiplexer which does to select only 8 outputs of one block to be coupled to the 8 inputs of the output bus couple ports. There are 3 output bus couple ports in which one is use to couple to the data bus of the PDC and two remained ports are used to couple to two remained read request sources. Data couple logic for the write request sources consist of only three 8 bit tristate output latch register 74 LS 373) and which are designed to be the byte multiplexer.

The Common Read Write Controller (CRWC) is designed to control the fuctions of the CPM by the typical dinamic memory control signals. In our design the CRWC is designed to generate the basic memory control signals on the base of 14 standard timing synchron pulses p0, ..., p12, p13 which are provided from the Memory Timing Logic (MTL) by multiplexing pulses d0, d1, ..., d13 to the pulses x0, x1, ..., x13 respectively.

The pulses d0, d1, ..., d13 are generated by D Timing Suorce and the pulses x0, x1, ..., x13 are generated by X Timing Suorce. When CPM to be shared by PDC, the T multiplexer does to select d0, d1, ..., d13 to be p0, p1, ..., p13 respectively, and when CPM to be shared by another memory request suorce the T multiplexer does to select the pulses x0, x1, ..., x13 to be p0, p1, ..., p13 respectively. Two timing suorses, D and X, are designed by the same way, each of them consists of one synchronous-devide by 14 counter, which is used to count the SCK pulse, and one 4 to 16 decoder, which is used to decode the output states of the counter. The differences in the design of two timing suorses are follows:

- The D Timing counter is designed to count continuously and synchronly with the CCK generated counter so that the leading edge of each CCK pulse always to be the falling edge of the d0 pulse.
- The X Timing counter is only enabled to count when any one of the X memory request suorses is accepted to service by the CPM and it only to count only 14 SCK pulses, from the state 0 to state 13. It is stopped to count when it reaches the state 13 until one of

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other request from any X request source to be accepted again.

Geometrically speaking, the standard timing syncron pulses d0, d1, ... d13 are used to sample each character column into 14 intervals with the width of each interval to be $\frac{1}{14}$ of the width of one character column, and also they are used to sample each character column of 64 character columns, from the 16th character column to the 79th character column, into 4 pixel columns with the width of each pixel column to be $\frac{1}{14}$ of the width of the character column.

The basic control logic of the CTC is designed to be 8 channels of "request in - wait - accept out" flag logic with respect to the assigned priority of each. 8 channels are indexed by X1, X2, X3, X4, X5, X6, X7, D with the assigned priorities from the highest to lowest are 1, 2, ... 7, 8 respectively. Also the channels X1, X2, X3, X4, X5, X6, X7, D are assigned to the memory request sources CDIC, CRFC, Z1Read, Z1Write, Z2Read, Z2Write, not used, PDC respectively. The PDC consists of 4 following logic stages:

- 8 Request Flag Registers X1RQ, X2RQ, ... X7RQ, DRQ
- 8 bit Latch Register (we used 74 LS 373)
- 8 to 3 Encoded Priority Logic (we used 74 LS 148)
- 3 to 8 Decoder (we used 74 LS 138)

7 first Request Flag Registers X1RQ, X2RQ, ... X7RQ are assigned to store 7 Request signal RQ1, RQ2, ... RQ7 which are provided by the request sources assigned to the channel X1, X2, ... , X7 respectively, with the output of each register is designed to be active low at the leading edge of the assigned Request pulse of it by connecting the RQ1, RQ2, ... , RQ7 to the clock pins of the X1RQ, X2RQ, ... , X7RQ respectively. Any of these 7 Request signals to be stored at the output Q of the respective register until the end of the memory cycle, which is performed to the answer that request. That means that when a source need to use the CPM, it generates a Request signal which to be stored at assigned request flag register all the time of waiting the accept from the CPM, and all the time of the accepting cycle, and that flag only to be cleared when that request will have been serviced completely by the CPM. In this manner, the pulse x12 to be used as the "X - End of Service" flag and the under service Request Flag Register to be cleared by this pulse.

The "D" Request Flag Register consists of two D flip-flops RD1 and RD2 is designed to work at SCK clock with D input of it to be connected to the DRQ signal of PDC, and it to be asynchronously cleared by any X Flag. RD2 is designed to delay the output of RD1,
by the leading edges of the pulses d10. The output of RD2 to be connected to the lowest priority input of the priority logic (channel D). By this way of designing the Display Read Request only to be accepted by the CPM any X Request source can to stop the display read operation at the end of the recent memory read cycle (at the leading edge of the nearest d10).

The effect of this design method on the CRT screen to be that 256 pixels of one pixel line may be not to display completely.

Table 1

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>RANGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vertical Blanking Time (VRIC)</td>
<td>900 μsec nominal</td>
</tr>
<tr>
<td>Vertical Drive Pulsewidth</td>
<td>300 μsec PW 1.4 ms</td>
</tr>
<tr>
<td>Horizontal Blanking Time (HRIC)</td>
<td>11 μsec nominal</td>
</tr>
<tr>
<td>Horizontal Drive Pulsewidth</td>
<td>25 μsec PW 30 μsec</td>
</tr>
<tr>
<td>Horizontal Repetition Rate</td>
<td>15,750 ± 500 pps</td>
</tr>
</tbody>
</table>
FIGURE 1

1a: Combining display block diagram
1b: Block diagram of High Speed Dot Timing Logic
1c: Dot Timing, DSTL timing diagram
Figure 2: Pictorial Display Controller (PDC) Block Diagram

Alpha numerical video

TOTAL SCREEN TIME = 340 PERIODS OF HRTC

(c) Displaying combination - screen timing diagram

(c) Displaying combination - line timing diagram
FIGURE 3: Hardware designing resolution of sharing the CPM
a/ Bloc diagram of the CPMs couple logic
b/ Bloc diagram of the CPM Trafic Controller-OTC