

AB L1&L2 v1.1.4 - 0.5mm, 5-layer Board with Microvias

Material Selection

Halogen-free FR-4
Permittivity @ 100MHz:
Permittivity @ 1GHz:
Loss Tangent @ 100MHz:
Loss Tangent @ 1GHz:
Lead Free Assembly Compatible

Solder resist colour: green Silkscreen print colour: white

Surface Finish

On top and bottom layer surfaces: electroless nickel immersion gold

Holes / Drilling

Drill files contain finished hole diameters Drilling layer pairs: 4-5, 1-5

Board Outline

Contour routed with break-away tabs

Element Counts (for reference only)

Components: 36
Nets: 79
Pads: 351
Tracks: 1671
Polygons: 19
Holes: 241
Vias: 214

Non-standard Tolerances

Holes sized 0.2mm may be plugged by plating. These are all vias. For them we do not care the finished hole sizes.

									Layer Name	Gerbe
Board Layer Stack						С	Orill Layer-Pairs	Top Overlay Top Solder Mask	.gto	
Cu 18um*	——————Prepreg	VT47-108	 30 60um	01				— O1 —	— Top Layer	.gtl
Cu 35um Cu 35um Cu 35um Cu 18um*		UT47	76um	02				— 02 ——	—— Plane 1 (GND)	. gp1
		UT47	 76um	03 04				— 03 — — 04 —	Mid Layer 1 Plane 2 (GND)	.g1 .gp2
	Prepreg	VT47-108	30 60um	05 —				— 05 —	— Bottom Layer	.gbl
* 25 (i	nal after	plating							Bottom Solder Mask	.gbs
*35um final after plating Total Laminated Thickness: 0.5mm +/- 0.05mm!									Bottom Overlay	. gbo
lotal L	aminated inickness: 0.5mm +/- 0.05m				- U.USMM !				Bottom Paste Mask	. gbp
									Board Outline	.gm1

Controlled Impedance Reference

Diff. trace width/space on bottom layer (microstrip) 75 ohms D10%: 0.125/0.1mm

Diff. trace width/space on top and bottom layer (microstrip) 60 ohms D10%: 0.175/0.1mm