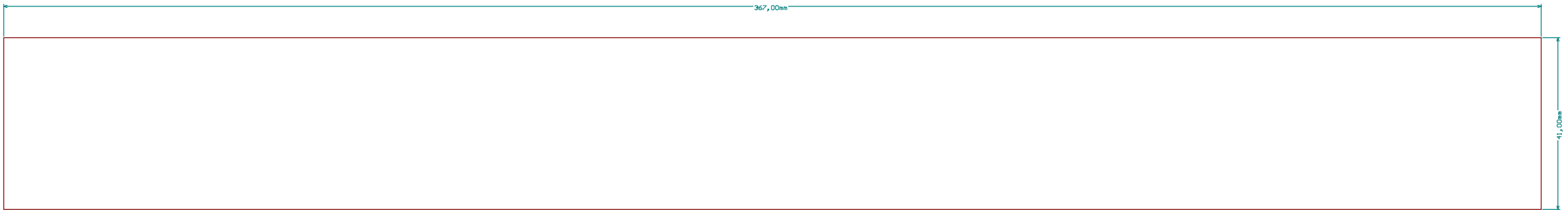

367,00mm
41,00mm

CB L1&L2 v1.3.1 - 0.5mm 5-Layer Board with Polyimide (VT901) Dielectric Layers and Blind Vias

Material Selection

Polyimide VT901
Permittivity @ 100MHz:
Permittivity @ 1GHz:
Loss Tangent @ 100MHz:
Loss Tangent @ 1GHz:
Lead Free Assembly Compatible

Solder resist colour: green
Silkscreen print colour: white

Surface Finish

On top and bottom layer surfaces:
electroless nickel immersion gold

Holes / Drilling

Drill files contain finished hole diameters
Drilling layer pairs: 1-2, 1-3, 1-5

Board Outline

Contour routed with break-away tabs

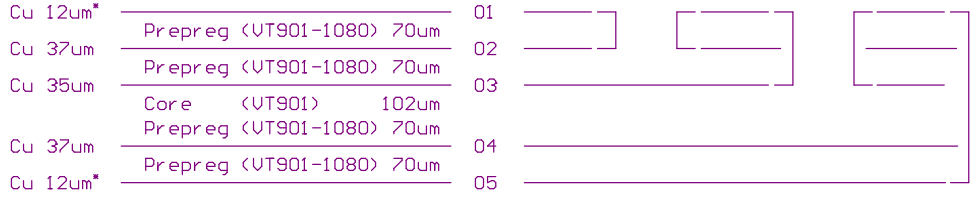
Element Counts
(for reference only)

Components:	165
Nets:	246
Pads:	1202
Tracks:	8057
Polygons:	61
Holes:	965
Vias:	912

Non-standard Tolerances

Holes sized 0.2mm may be plugged by plating. These are all vias.
For them we do not care the finished hole sizes.

Board Layer Stack



*37um final after plating
Total Laminated Thickness: 0.5mm

Drill Layer-Pairs

Layer Name	Gerber
Top Paste Mask	.gtp
Top Overlay	.gto
Top Solder Mask	.gts
Top Layer	.gtl
Plane 1 (GND)	.gp1
Mid Layer 1	.g1
Mid Layer 2 (PWR)	.g2
Bottom Layer (PWR)	.gbl
Bottom Solder Mask	.gbs
Board Outline	.gm1

Controlled Impedance Reference

Diff. trace width/space on middle layer1 (stripline) 75 ohms +/- 10% : 0.100/0.100mm.
Diff. trace width/space on middle layer1 (stripline) 60 ohms +/- 10% : 0.150/0.100mm.
Diff. trace width/space on top layer (microstrip) 75 ohms +/- 10% : 0.125/0.100mm.
Diff. trace width/space on top layer (microstrip) 60 ohms +/- 10% : 0.200/0.100mm.